MF610
Single-Phase BLDC Motor Controller
Datasheet

Version 0.06 – Oct. 8, 2024

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Revision History

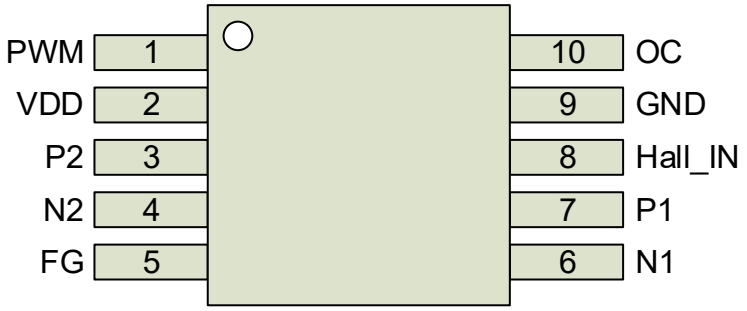
Revision	Date	Description
0.04	2021/01/15	Add pin description
0.05	2023/08/17	1. Updated “IMPORTANT NOTICE” 2. Updated DC/AC Characteristics: f_{SYS}, I_{OP}, V_{BRD}, V_{BG}, f_{IHRC}, V_{ADC} and ADclk 3. Amend chapter 4 (three-phase diagram)
0.06	2024/10/08	1. Modify the maximum voltage of VDD to 6.5V 2. Add a note that the time from 6V to 6.5V must be less than 25us

1. Key Features

- Single-phase BLDC motor with hall IC interface
- PWM or voltage control input
- FG/RD/ALM/RALN/RXX/RRXX output
- Close loop or/and open loop control
- Current limit and over-current protection
- Soft-start, lock-protect and auto-restart
- System protection
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
- MTP Programming
  - Support 6-wire factory programming mode
  - Support 4-wire in-system programming mode
- DC Fan Applications
  - Operating voltage range: 3.5V~6.5V
  - Operating temperature range: -40°C~105°C
- Package Information
  - MF610-M10: MSOP10 (118mil)

MF610 is a single phase BLDC motor controller based on 8-bit 8-FPPA MCU which can be programmed by 6-wire factory mode or 4-wire ISP mode. MF610 receives motor position signal from Hall IC and can control the H-bridge flexibly to make the best efficiency of the motor. Through the PADAUK patented AP development system, it can easily set any speed curve, output signal and protection parameters etc., and it can observe the motor response online immediately. Using the MF610's development system, it's much easier and adjustable for application.

2. Pin Diagram and Pin Description



MF610: M10 (MSOP10-118mil)

Pin Name	I/O	Description
PWM/ PB7	Input	PWM signal input
VDD	-	Power pin. **Needs a 1uF and a 0.1uF capacitor in parallel.**
P2/ PA6	Output	Output signal to control the high side of motor driver
N2/ PA7	Output	Output signal to control the low side of motor driver
FG/ PA0	Output	Rotation speed signal output
N1/ PA3	Output	Output signal to control the low side of motor driver
P1/ PA4	Output	Output signal to control the high side of motor driver
Hall_IN/ PA5	Input	Digital hall signal input
GND	-	Ground
OC/ PB0	Input	Analog input to sense motor current

3. Device Characteristics

3.1. Absolute Maximum Ratings

Name	Min	Typ.	Max	Unit	Notes
Supply Voltage (VDD)	3.5		6.5	V	**Exceed the maximum rating may cause permanent damaged!! The time of the VDD voltage between 6V and 6.5V must be less than 25us**
Input Voltage	-0.3		V_{DD} + 0.2	V	
Operating Temperature	-40		105	°C	
Storage Temperature	-50		125	°C	
Junction Temperature		150		°C	

3.2. DC/AC Characteristics

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{DD}	Operating Voltage	3.5 4.75	5.0 5.0	6.5 6.5	V	-40 °C <Ta<85 °C -40 °C <Ta<105 °C
V_{FSV}	Forbidden V_{DD} startup voltage range	0.7		1.6	V	
V_{PORV}	V_{DD} power down release voltage			0.7	V	
T_{POR}	V_{DD} power on time (V_{DD} from 0V to 5V)			50	ms	
T_{FSV}	V_{DD} power on time during V_{FSV} range			10	ms	
f_{SYS}	System clock IHRC/2	0		8M	Hz	V_{DD} = 3.3V
I_{OP}	Operating Current		3.5		mA	f_{SYS}=8MIPS@5.0V
I_{PD}	Power Down Current (by ***stopsys*** command)		3 1		uA uA	V_{DD}=5.0V V_{DD}=3.3V
I_{PS}	Power Save Current (by ***stopexe*** command)		0.4		mA	VDD=5.0V; Bandgap, LVD, IHRC, ILRC, Timer16 modules are ON.
V_{IL}	Input low voltage for IO lines	0		0.2V_{DD}	V	
V_{IH}	Input high voltage for IO lines	0.8 V_{DD}		V_{DD}	V	
I_{OL}	IO lines sink current	11	14	17	mA	V_{DD}=5.0V, V_{OL}=0.5V
I_{OH}	IO lines drive current	-8	-10	-12	mA	V_{DD}=5.0V, V_{OH}=4.5V
R_{PH}	Pull-high Resistance		90 170		KΩ	V_{DD}=5.0V V_{DD}=3.3V

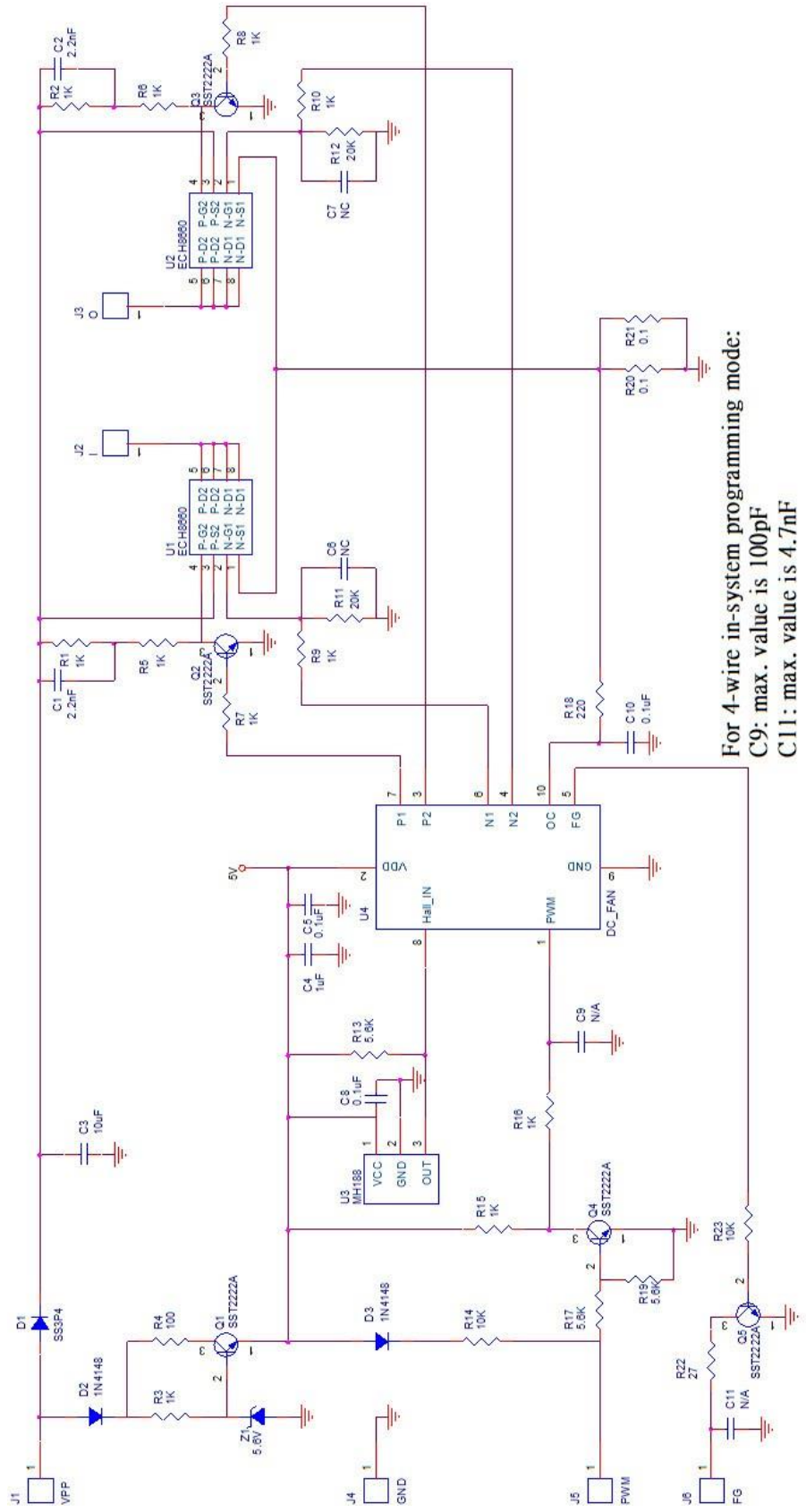
Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
V_{BRD}	Low Voltage Detect Voltage * (Brown-out voltage)	3.0	3.3	3.5	V	
V_{BG}	Bandgap Reference Voltage (before calibration)	1.12	1.20	1.28	V	V_{DD}=5V, 25°C
	Bandgap Reference Voltage * (after calibration)	1.17*	1.20*	1.23*		V_{DD}=3.3V ~ 5.5V, -40°C <Ta<105°C*
f_{IHRC}	Frequency of IHRC after calibration *	15.52*	16*	16.48*	MHz	25°C, V_{DD}=3.3V~5.5V
		14*	16*	17.28*		V_{DD}=3V~5.5V, -40°C <Ta<105°C*
f_{ILRC}	Frequency of ILRC *	31.5*	33.8*	35*	KHz	V_{DD}=5.0V, Ta=25°C
		29*	33.8*	38.4*		V_{DD}=5.0V, -40°C <Ta<85°C*
		32*	34*	35.5*		V_{DD}=3.3V, Ta=25°C
		29*	34*	40*		V_{DD}=3.3V, -40°C <Ta<85°C*
V_{ADC}	Workable ADC operating Voltage	3.3		6.5	V	
V_{AD}	AD Input Voltage	0		V_{DD}	V	
ADrs	ADC resolution			11	bit	
ADclk	ADC clock period		2		us	3.3V ~ 5.5V
t_{ADCONV}	ADC conversion time (T_{ADCLK} is the period of the selected AD conversion clock)		14		T_{ADCLK}	
AD DNL	ADC Differential NonLinearity		±3*		LSB	
AD INL	ADC Integral NonLinearity		±3*		LSB	
ADos	ADC offset*		3 4		LSB	-40°C <Ta<85°C* -40°C <Ta<105°C*
t_{INT}	Interrupt pulse width	30			ns	V_{DD} = 5.0V
V_{DR}	RAM data retention voltage*	1.5			V	In power-down mode.
t_{WDT}	Watchdog timeout period (T_{ILRC} is the clock period of ILRC)		4096			misc[1:0]=01
			16384			misc[1:0]=10
t_{SBP}	System boot-up period from power-on		1024		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC

Symbol	Description	Min	Typ	Max	Unit	Conditions (Ta=25℃)
t_{WUP}	System wake-up period					
	Fast wake-up by IO toggle from STOPEXE suspend		128		T_{SYS}	Where T_{SYS} is the time period of system clock
	Fast wake-up by IO toggle from STOPSYS suspend, IHRC is the system clock		128 T_{SYS} + T_{SIHRC}			Where T_{SIHRC} is the stable time of IHRC from power-on.
	Fast wake-up by IO toggle from STOPSYS suspend, ILRC is the system clock		128 T_{SYS} + T_{SILRC}			Where T_{SILRC} is the stable time of ILRC from power-on.
	Normal wake-up from STOPEXE or STOPSYS suspend		1024		T_{ILRC}	Where T_{ILRC} is the clock period of ILRC
HCPos	Comparator offset*	-	±10	±20	mV	
HCPcm	Comparator input common mode*	0		V_{DD}-1.5	V	
HCPspt	Comparator response time**		100	500	ns	Both Rising and Falling
HCPmc	Stable time to change comparator mode		2.5	7.5	us	

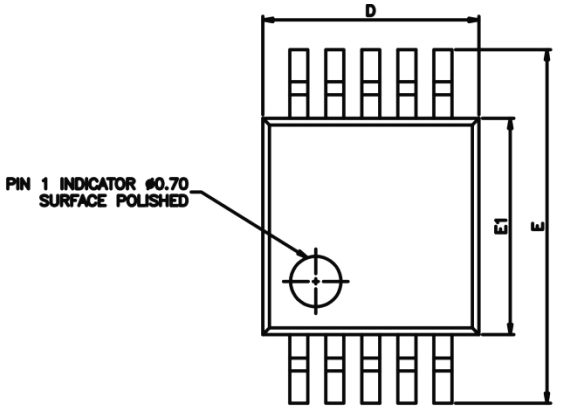
*These parameters are for design reference, not tested for every chip.
** Response time is measured with comparator input at (V_{DD}-1.5)/2 -100mV, and (V_{DD}-1.5)/2+100mV

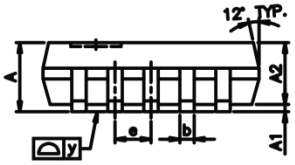
The characteristic diagrams are the actual measured values. Considering the influence of production drift and other factors, the data in the table are within the safety range of the actual measured values.

4. Reference Application Circuit

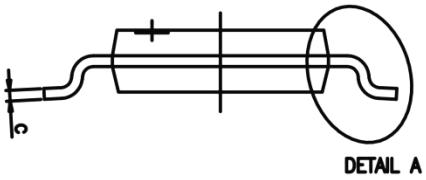


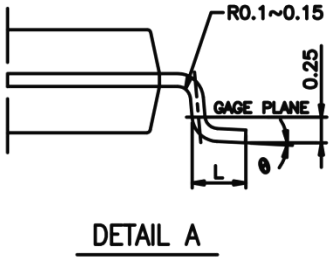
5. Package Information: MSOP10 (118mil)





SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.86	0.95
b	0.17	0.20	0.27
c	0.08	0.15	0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	—	0.50	—
L	0.40	0.53	0.80
y	—	—	0.076
θ	0°	3°	8°





NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : OLIN C7025
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.005"[0.12mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MO-187